What is claimed is:

1. A method of fabricating a submicron semiconductor device comprising:

forming an oxide layer on a substrate;

forming a polysilicon layer on said oxide layer;

forming a hard mask on said polysilicon layer;

depositing a photoresist on said hard mask and patterning said hard mask by using said photoresist; and

etching said polysilicon layer using a pattern embodied by said hard mask, wherein said etching undercuts said polysilicon layer to form a feature in said polysilicon layer having a critical dimension smaller than a corresponding critical dimension in said hard mask.

2. The method according to claim 1, further comprising depositing an ARC on said hard mask so as to lower reflectivity.

3. The method according to claim 2, wherein said ARC is of organic or inorganic material.

4. The method according to claim 1, wherein said photoresist patterning is performed using a KrF laser as a light source.

5. The method according to claim 1, wherein said hard mask is a SiH_4 oxide deposited by means of PE-CVD.

6. The method according to claim 1, wherein said hard mask has a thickness of about 150~400Å.

7. The method according to claim 1, wherein said pattern embodied by said hard mask is formed by etching said hard mask using said photoresist patterned as an etching mask.

8. The method according to claim 7, wherein said hard mask is etched by means of isotropic etching.

9. The method according to claim 8, wherein said isotropic etching is plasma etching.

10. The method according to claim 9, wherein said plasma etching uses SF_6 gas as an etching gas.

11. The method according to claim 1, wherein said etching is performed through plasma etching.

12. The method according to claim 11, wherein said plasma etching is performed using Cl_2/HBr, Cl_2/O_2 or HBr/O_2 as an etching gas so that the selectivity of said polysilicon to said oxide can be about 10 to 1.

13. A method of fabricating a submicron semiconductor device comprising:

forming an oxide layer on a substrate;

forming a polysilicon layer on said oxide layer;

forming a hard mask on said polysilicon layer;

depositing a photoresist on said hard mask and patterning said hard mask by using said photoresist;

etching said polysilicon layer using a pattern embodied by said hard mask; and

selectively removing said hard mask using a wet etch while protecting said polysilicon layer and said oxide layer from etching.

14. The method according to claim 13, further comprising depositing an ARC on said hard mask so as to lower reflectivity.

15. The method according to claim 13, wherein said removing of hard mask is performed through wet etching by HF gas, which is generated gasifying a solution of about 39% HF, at the same time that said gas protects a polysilicon gate and a gate oxide.

16. The method according to claim 15, wherein said HF gas is formed through spraying N_2 gas onto the surface of a chemical bath containing HF solution.

17. The method according to claim 13, wherein said wet-etching is performed on a hot plate having a temperature of about 50~90℃.

18. The method according to claim 13, wherein an etching rate of said wet-etching is less than about 1Å/min for said gate oxide and more than about 200Å/min for said hard mask.

19. The method according to claim 13, wherein said photoresist patterning is performed using a KrF Laser as a light source.